A Scalable Heterogeneous Multicore Architecture for ADAS

Presented at HOT CHIPS: A Symposium on High Performance Chips

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Zoran Nikolić*

Rama Venkatasubramanian*

Jason A.T. Jones*

Peter Labaziewicz*

*Embedded Processing Business Unit, Texas Instruments Inc.

Presentation Overview

- Agenda
  - Highlight challenges of implementing Advanced Driver Assistance Systems (ADAS) in embedded systems
  - Discuss ADAS system options and compromises
  - High level overview of TDAx SOC
  - Mapping ADAS use cases to devices from TDAx SOC families

Worldwide Road Traffic Fatalities

Total 2004

Leading Cause	%
1. Ischemic heart disease	12.2
2. Cerebrovascular disease	9.7
3. Lower respiratory infections	7.0
4. Chronic obstructive pulmonary disease	5.1
5. Diarrheal diseases	3.6
6. HIV	3.5
7. Tuberculosis	2.5
8. Trachea, bronchus, lung cancers	2.3
9. Road traffic injuries	**2.2**
10. Prematurity and low birth weight	2.0

1.3 million

~2 million

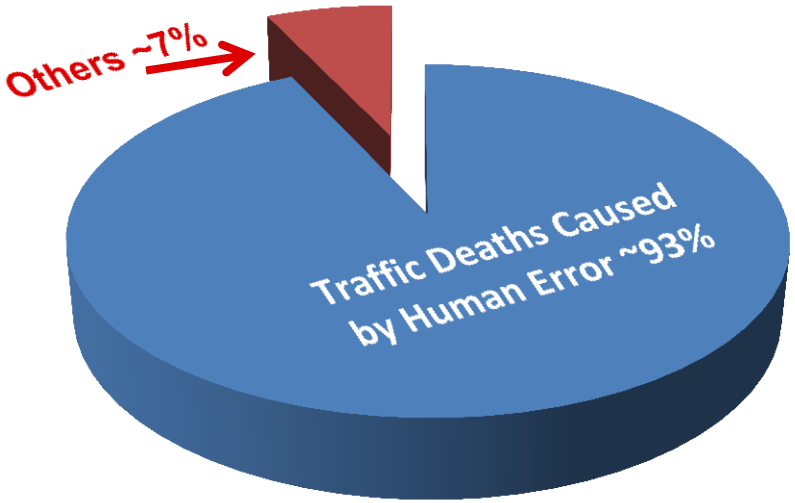
Total 2030

Leading Cause	%
1. Ischemic heart disease	14.2
2. Cerebrovascular disease	12.1
3. Chronic obstructive pulmonary disease	8.0
4. Lower respiratory infections	3.8
5. Road traffic injuries	**3.6**
6. Trachea, bronchus, lung cancers	3.4
7. Diabetes mellitus	3.3
8. Hypertensive heart disease	2.1
9. Stomach cancer	1.9
10. HIV	1.8

Source World Health Organization

Eliminating Human Error Can Save Lives

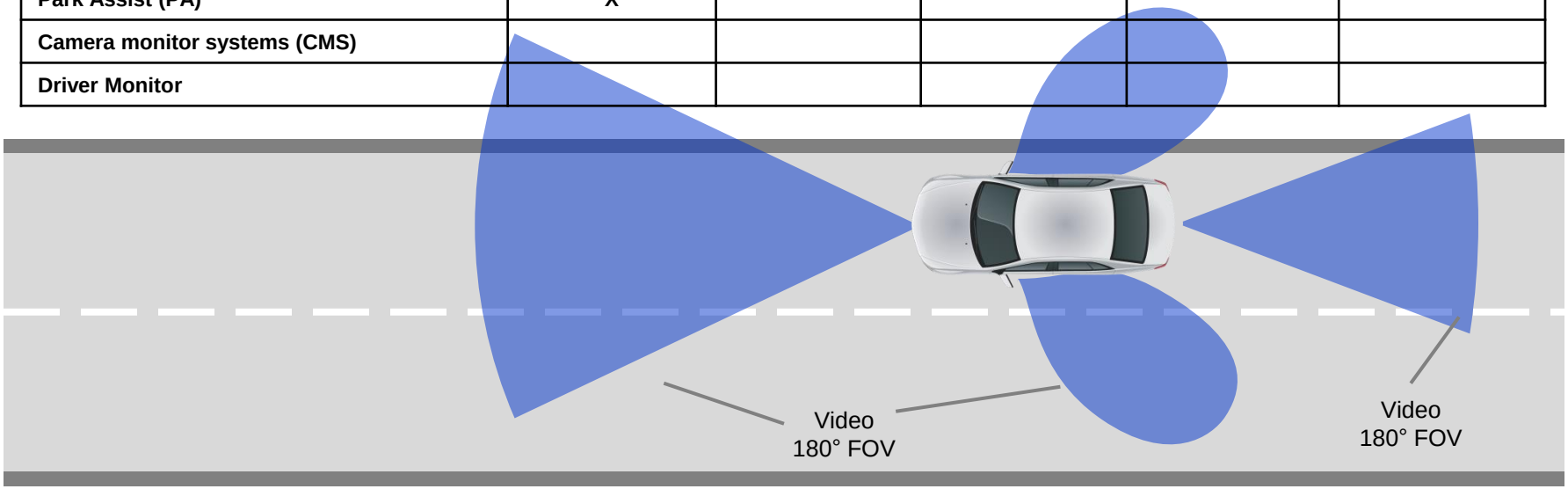
- According to Tri-Level Study of the Causes of Traffic Accidents published by NHTSA in 1979, "human errors and deficiencies" are a definite or probable cause in 90-93% of the incidents examined.
- By eliminating human errors that cause traffic accidents ADAS can save lives, reduce severity of injuries and reduce property damage



Source NHTSA

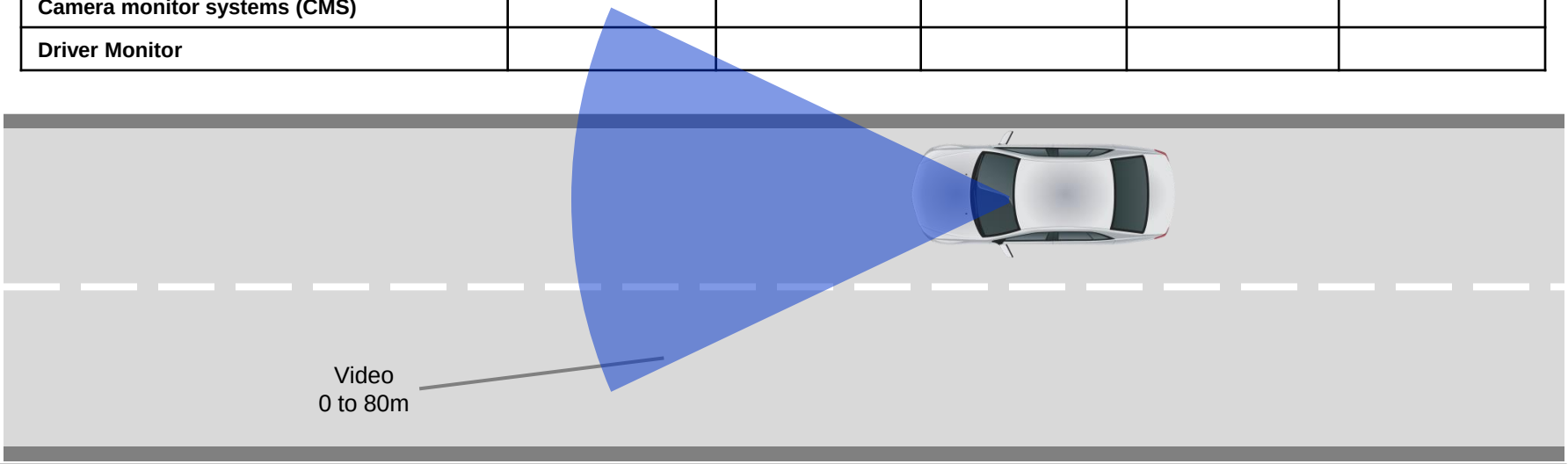
ADAS Surround View - Applications Summary

Application \ Sensor Type	Vision	Infrared	Long Range Radar 76..81MHz	Short / Mid Range Radar 24..26 / 76..81 GHz	Lidar
Adaptive Front Lighting (AFL), Traffic Sign Recognition (TSR)					
Night vision (NV)					
Adaptive Cruise Control (ACC)					
Lane Departure Warning (LDW)					
Low-Speed ACC, Emergency Brake Assist (EBA), Lane Keep Support (LKS)					
Pedestrian detection	X				
Blind Spot Detection (BSD), Rear Collision Warning (RCW), Cross Traffic Alert (CTA)	X				
Park Assist (PA)	X				
Camera monitor systems (CMS)					
Driver Monitor					



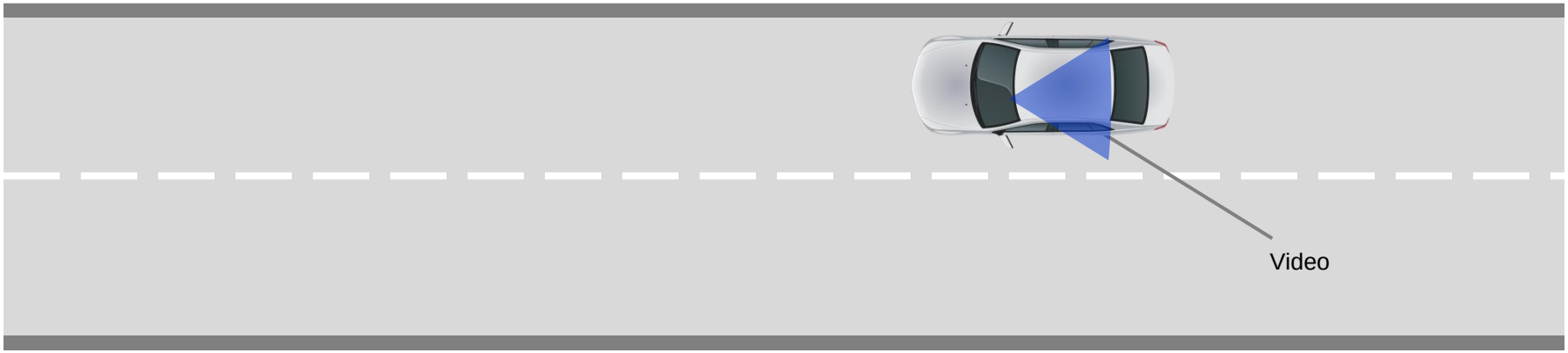
ADAS Front Camera - Applications Summary

Sensor Type / Application	Vision	Infrared	Long Range Radar 76..81MHz	Short / Mid Range Radar 24..26 / 76..81 GHz	Lidar
Adaptive Front Lighting (AFL), Traffic Sign Recognition (TSR)	**X**				
Night vision (NV)					
Adaptive Cruise Control (ACC)	X				
Lane Departure Warning (LDW)	**X**				
Low-Speed ACC, Emergency Brake Assist (EBA), Lane Keep Support (LKS)	X				
Pedestrian detection	**X**				
Blind Spot Detection (BSD), Rear Collision Warning (RCW), Cross Traffic Alert (CTA)					
Park Assist (PA)					
Camera monitor systems (CMS)					
Driver Monitor					



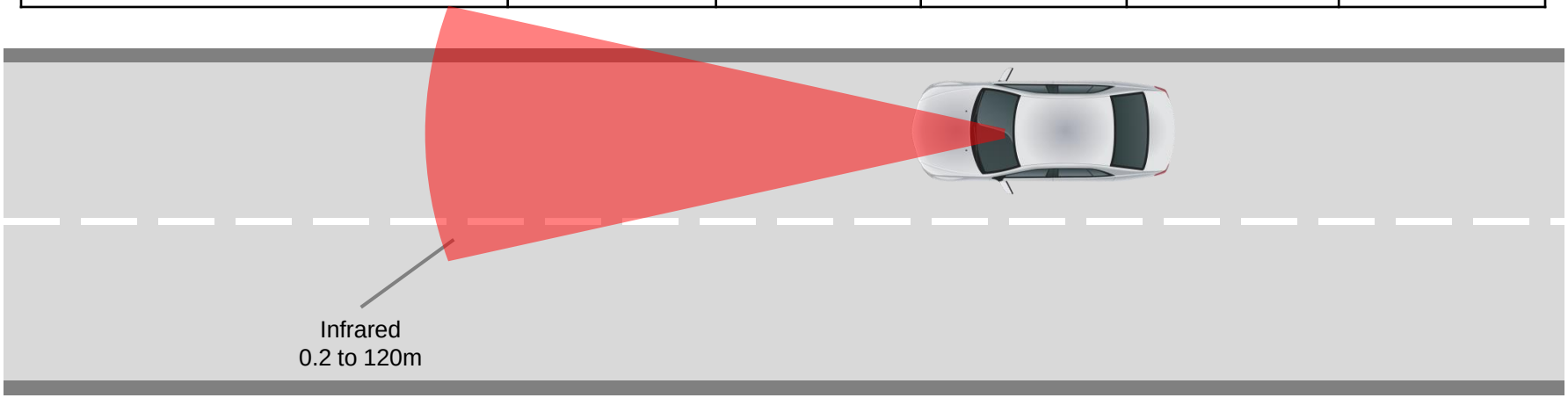
ADAS Driver Monitor

Sensor Type / Application	Vision	Infrared	Long Range Radar 76..81MHz	Short / Mid Range Radar 24..26 / 76..81 GHz	Lidar
Adaptive Front Lighting (AFL), Traffic Sign Recognition (TSR)					
Night vision (NV)					
Adaptive Cruise Control (ACC)					
Lane Departure Warning (LDW)					
Low-Speed ACC, Emergency Brake Assist (EBA), Lane Keep Support (LKS)					
Pedestrian detection					
Blind Spot Detection (BSD), Rear Collision Warning (RCW), Cross Traffic Alert (CTA)					
Park Assist (PA)					
Camera monitor systems (CMS)					
Driver Monitor	X				



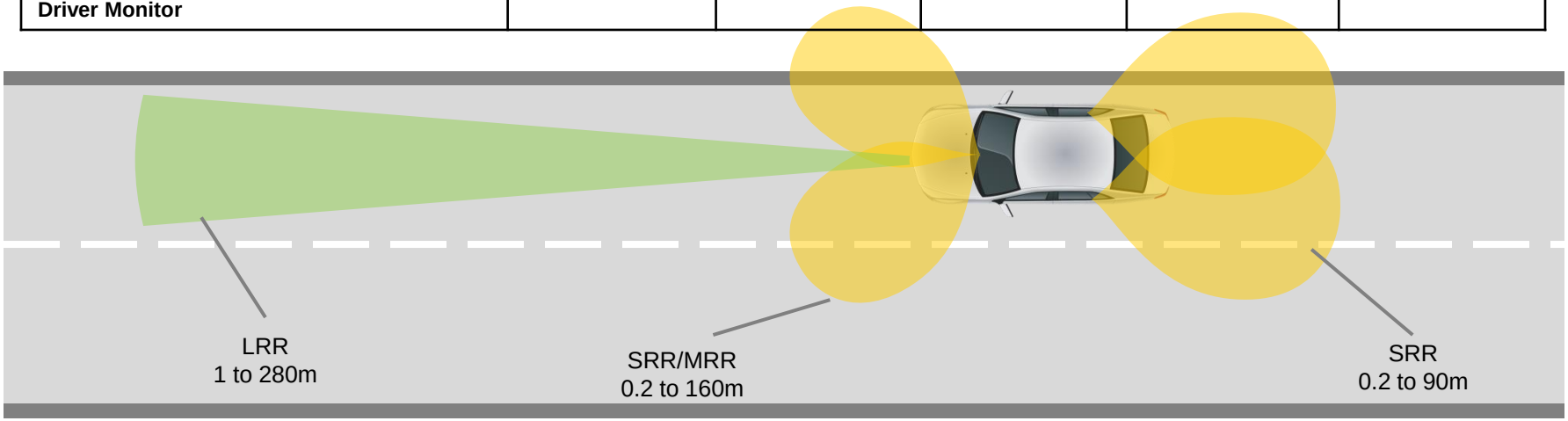
ADAS Night Vision Applications Summary

Sensor Type / Application	Vision	Infrared	Long Range Radar 76..81MHz	Short / Mid Range Radar 24..26 / 76..81 GHz	Lidar
Adaptive Front Lighting (AFL), Traffic Sign Recognition (TSR)					
Night vision (NV)		X			
Adaptive Cruise Control (ACC)					
Lane Departure Warning (LDW)					
Low-Speed ACC, Emergency Brake Assist (EBA), Lane Keep Support (LKS)					
Pedestrian detection		X			
Blind Spot Detection (BSD), Rear Collision Warning (RCW), Cross Traffic Alert (CTA)					
Park Assist (PA)					
Camera monitor systems (CMS)					
Driver Monitor					



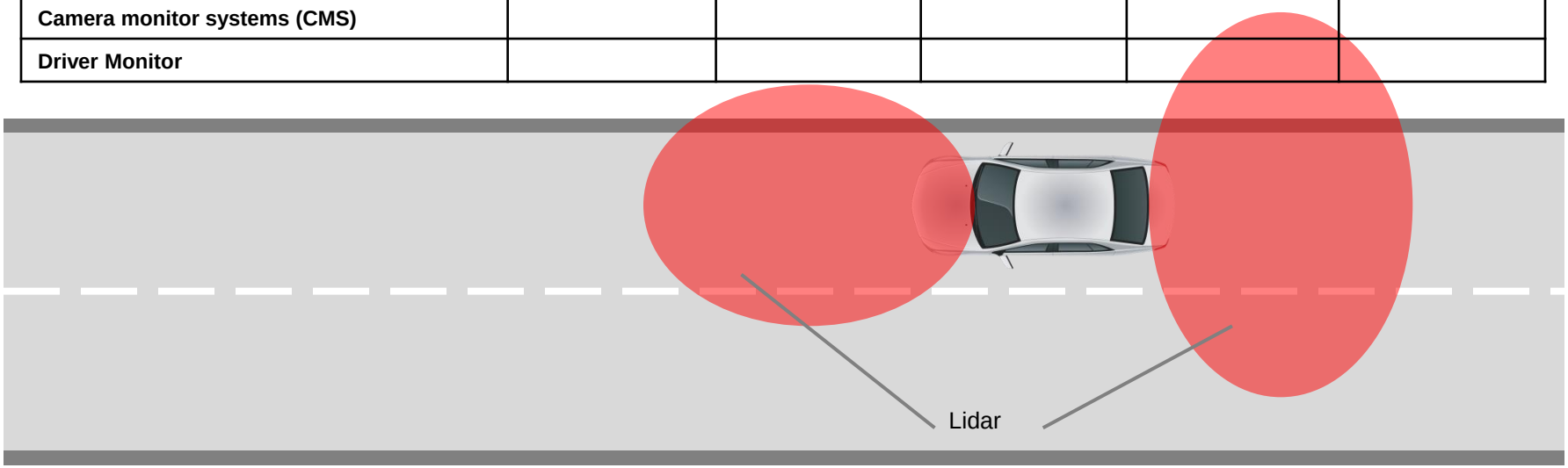
ADAS Radar Applications Summary

Sensor Type / Application	Vision	Infrared	Long Range Radar 76..81MHz	Short / Mid Range Radar 24..26 / 76..81 GHz	Lidar
Adaptive Front Lighting (AFL), Traffic Sign Recognition (TSR)					
Night vision (NV)					
Adaptive Cruise Control (ACC)			X	X	
Lane Departure Warning (LDW)					
Low-Speed ACC, Emergency Brake Assist (EBA), Lane Keep Support (LKS)				X	
Pedestrian detection				X	
Blind Spot Detection (BSD), Rear Collision Warning (RCW), Cross Traffic Alert (CTA)				X	
Park Assist (PA)				X	
Camera monitor systems (CMS)					
Driver Monitor					



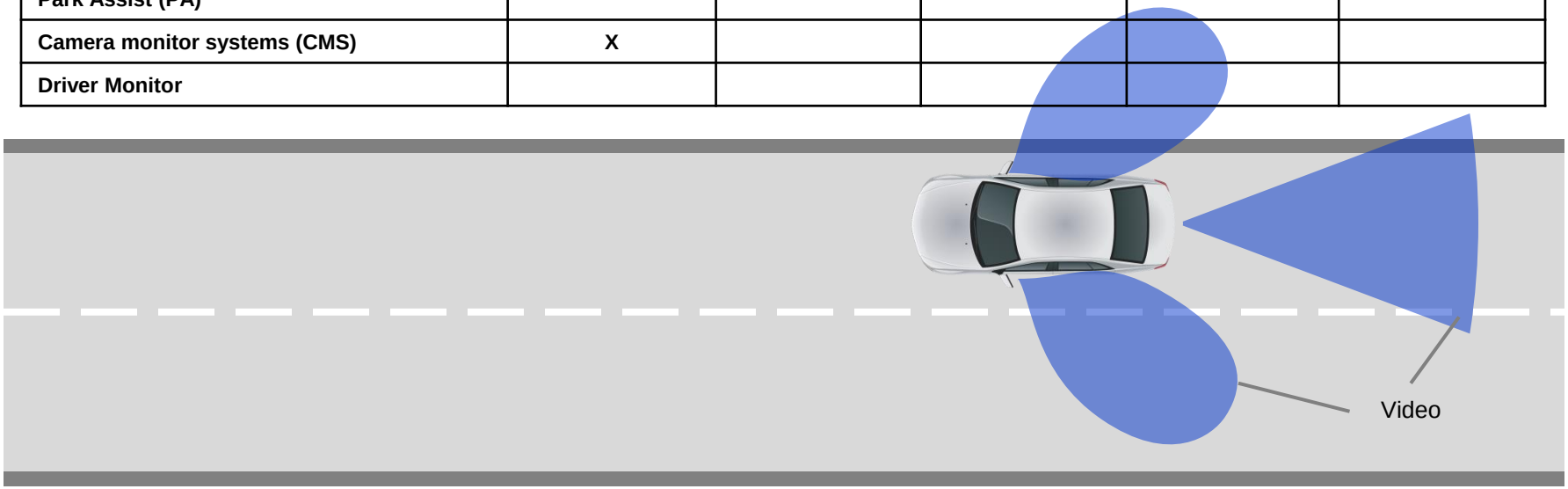
ADAS Lidar Applications Summary

Sensor Type / Application	Vision	Infrared	Long Range Radar 76..81MHz	Short / Mid Range Radar 24..26 / 76..81 GHz	Lidar
Adaptive Front Lighting (AFL), Traffic Sign Recognition (TSR)					
Night vision (NV)					
Adaptive Cruise Control (ACC)					X
Lane Departure Warning (LDW)					
Low-Speed ACC, Emergency Brake Assist (EBA), Lane Keep Support (LKS)					**X**
Pedestrian detection					
Blind Spot Detection (BSD), Rear Collision Warning (RCW), Cross Traffic Alert (CTA)					X
Park Assist (PA)					X
Camera monitor systems (CMS)					
Driver Monitor					

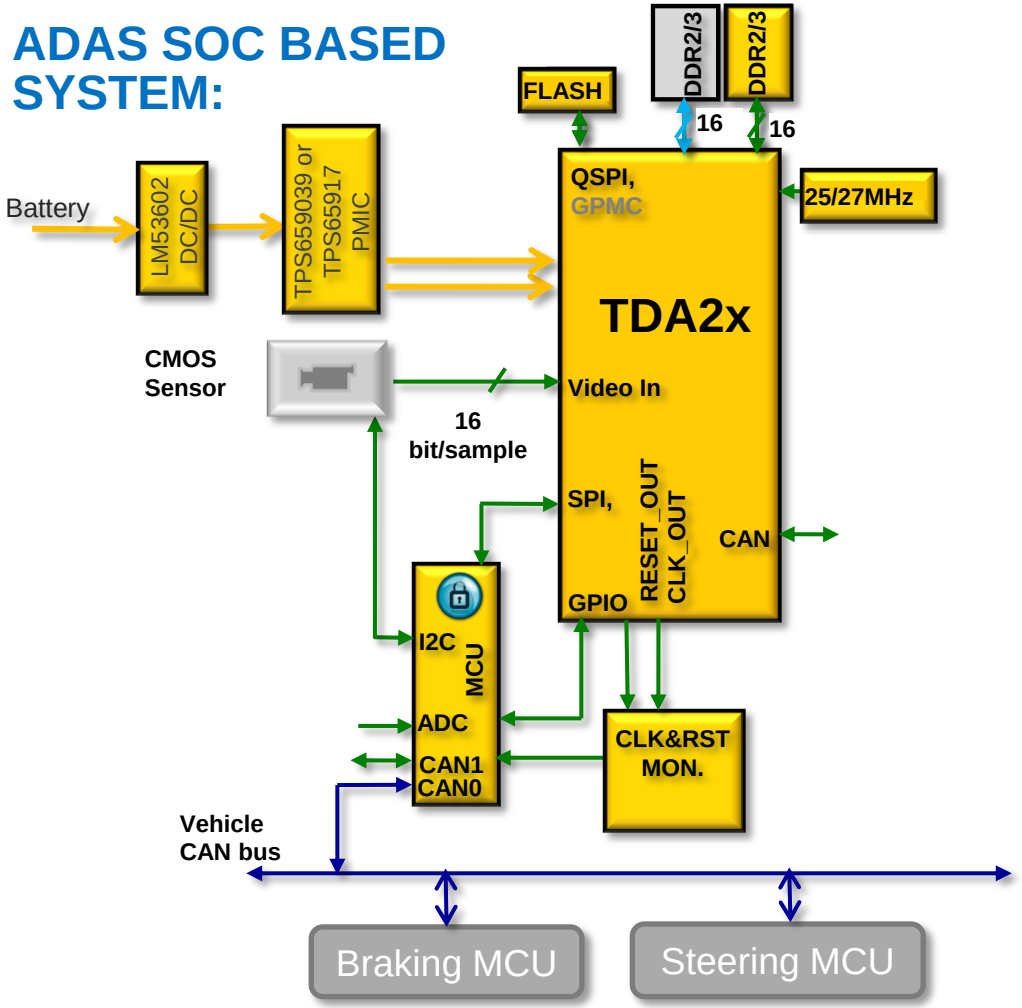


ADAS CMS- Applications Summary

Sensor Type / Application	Vision	Infrared	Long Range Radar 76..81MHz	Short / Mid Range Radar 24..26 / 76..81 GHz	Lidar
Adaptive Front Lighting (AFL), Traffic Sign Recognition (TSR)					
Night vision (NV)					
Adaptive Cruise Control (ACC)					
Lane Departure Warning (LDW)					
Low-Speed ACC, Emergency Brake Assist (EBA), Lane Keep Support (LKS)					
Pedestrian detection					
Blind Spot Detection (BSD), Rear Collision Warning (RCW), Cross Traffic Alert (CTA)					
Park Assist (PA)					
Camera monitor systems (CMS)	X				
Driver Monitor					

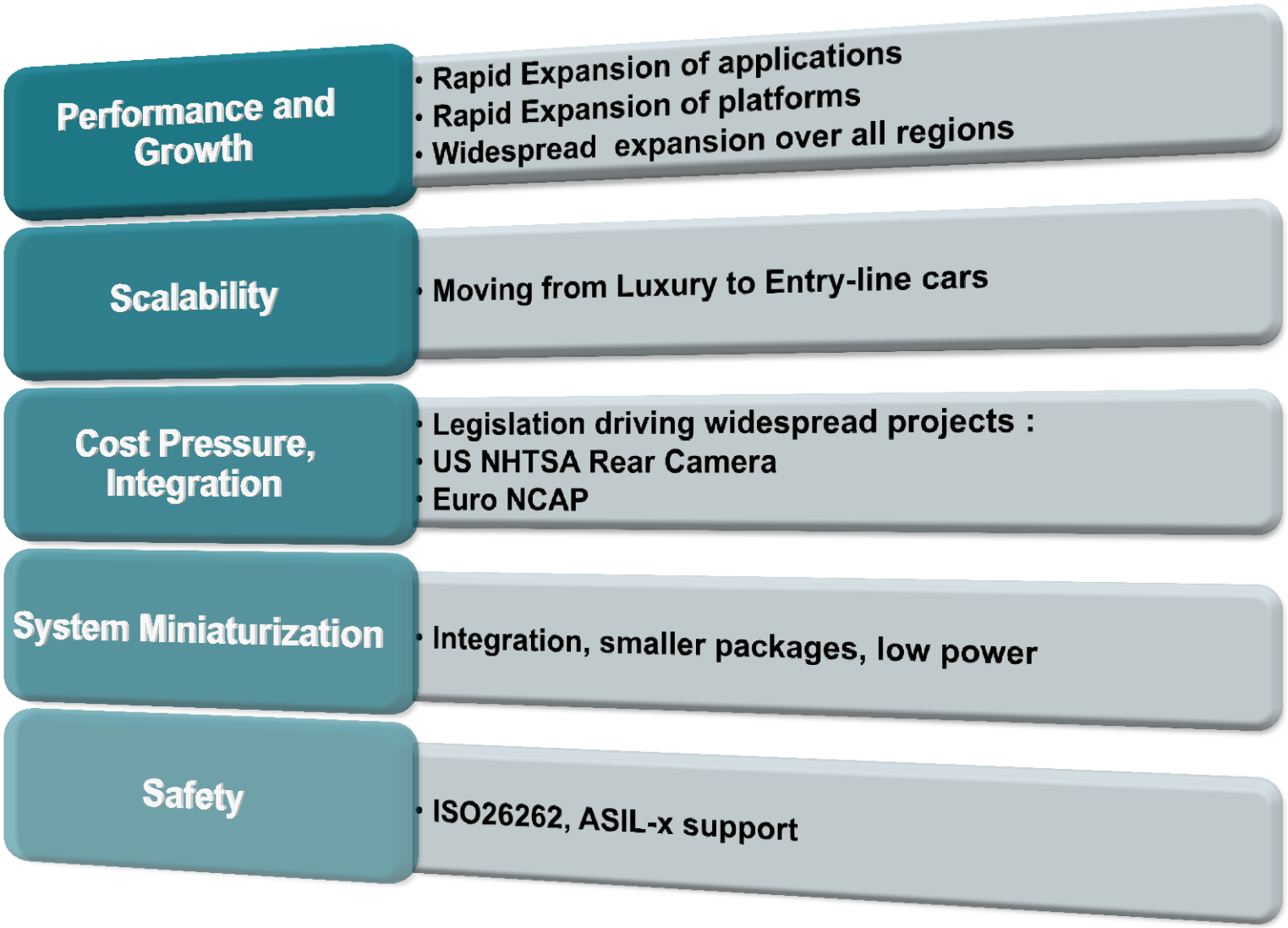


Mono Front Camera Block Diagram



- Compute performance increase must come without compromising overall system cost.
- The system needs to be packaged in a miniature enclosure and must deliver maximum compute performance while dissipating minimum heat in order to operate at the extreme temperatures.
- The opposing requirements create a very challenging environment.

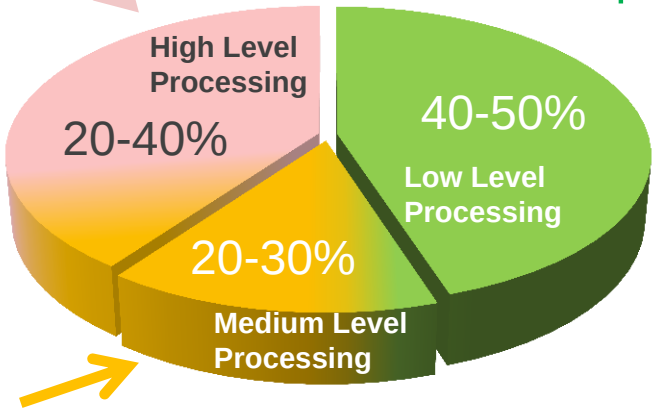
ADAS Market Trends



Various Stages of ADAS Vision Applications

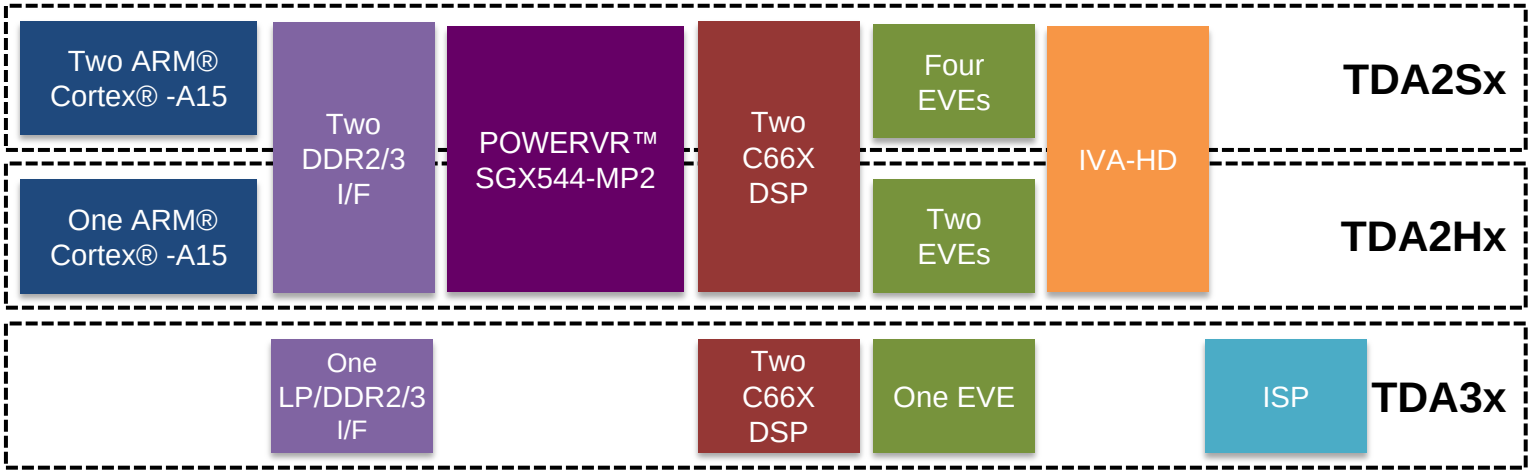
- High-level processing is typically responsible for decision making and tracking and takes input from previous processing stages.

- Low level processing is characterized by repetitive operations at pixel level requiring high computational requirements and memory bandwidth. Low level processing is typically best served by applying single instruction on multiple data (SIMD).



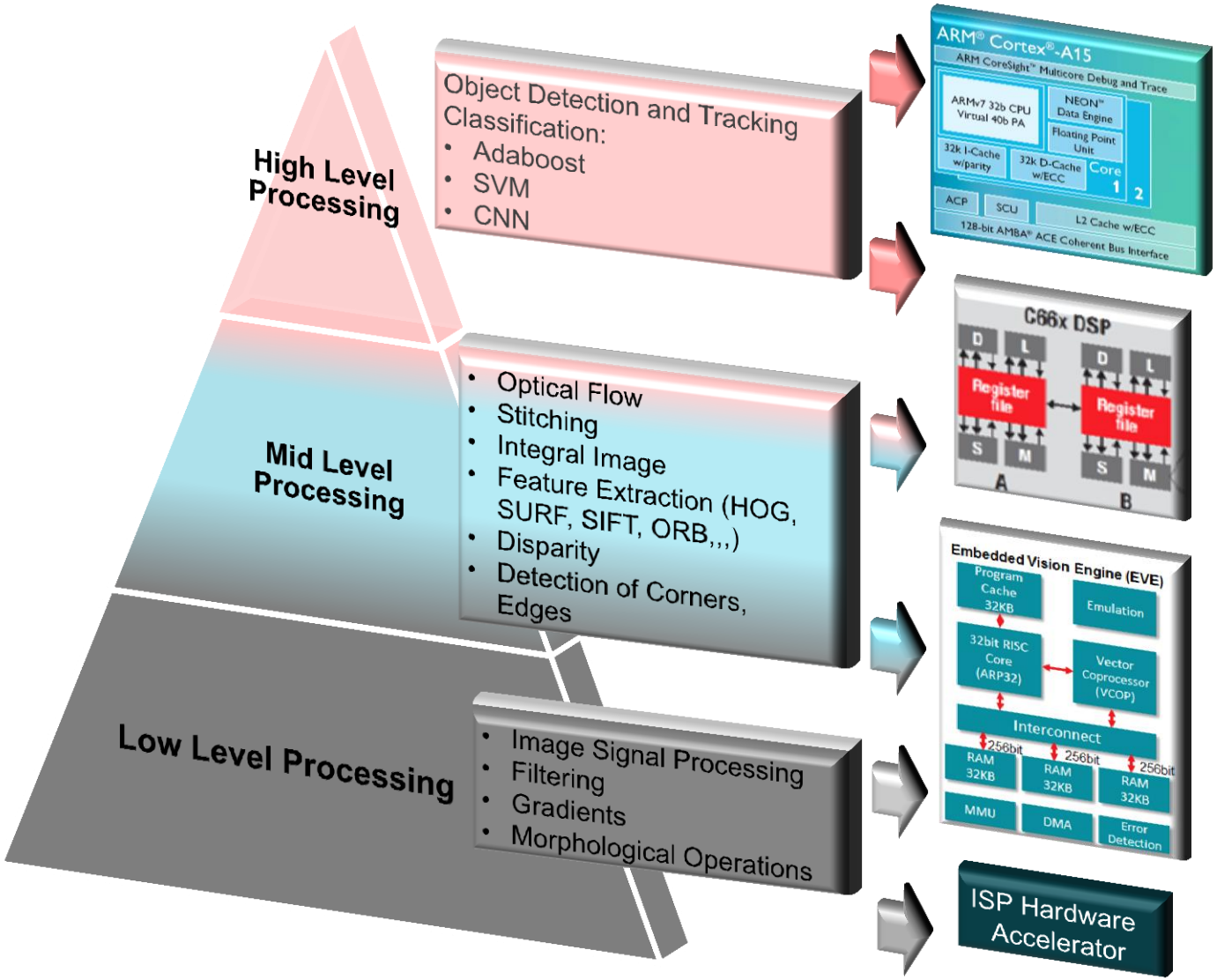
- Mid level Processing has focus on certain objects or regions of interest that meet particular classification criteria (mid-level processing). Mid-level vision is typically best served by using some combination of SIMD and multiple instructions on multiple data (MIMD).

The TDA SoC Family Architecture



- One platform multiple HW and SW compatible products

TDAx Processing Pipeline Support through Optimized Heterogeneous Architecture



ARM/DSP for Control & High-level vision stages

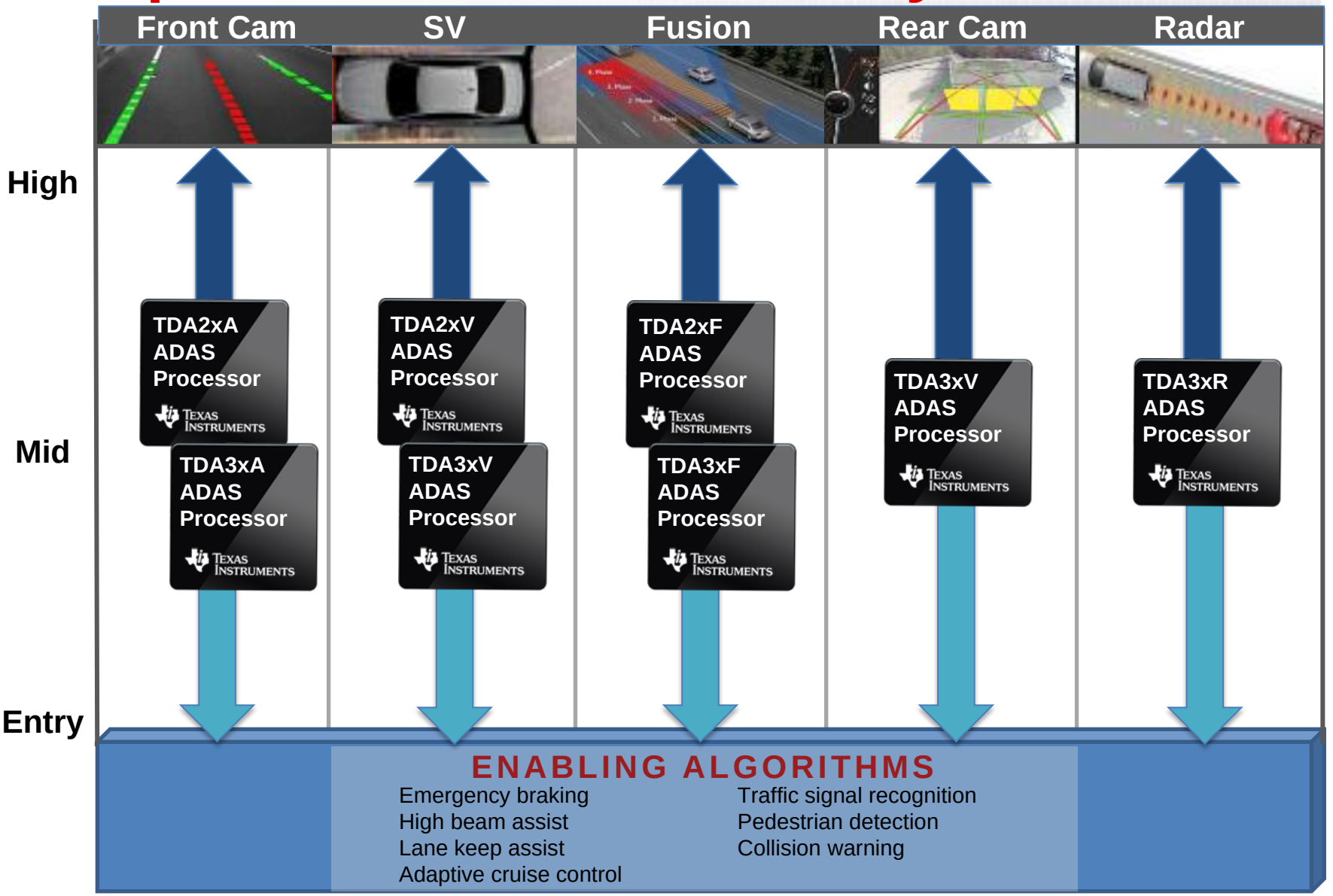
ARM Cortex A or M:
Scalable RISC
Data Fusion
Memory Coherency

DSP:
VLIW SIMD+MIMD
Data Fusion

EVE Vector Coprocessor:
High Bandwidth Pixel Operations
SIMD Parallelism
Energy Efficiency

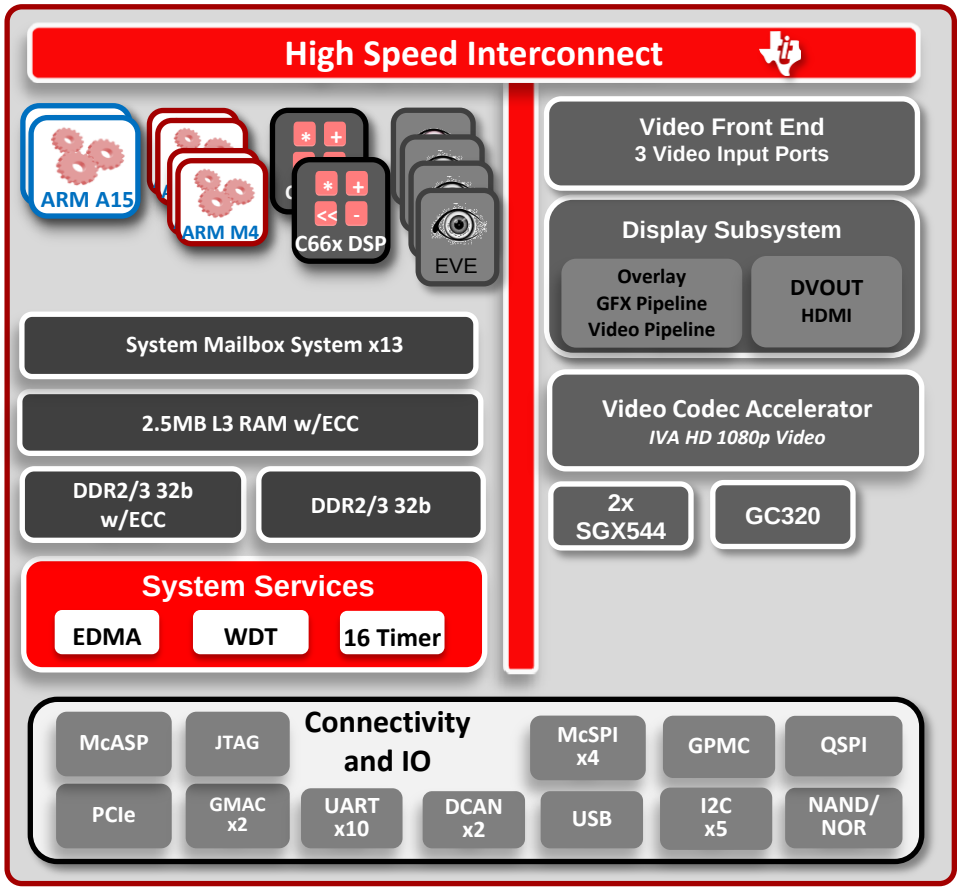
Hardware Acceleration:
High Bandwidth Pixel Operations
Configurable HW Acceleration

Complete HW & SW Scalability



TDA2x scalable family (superset)

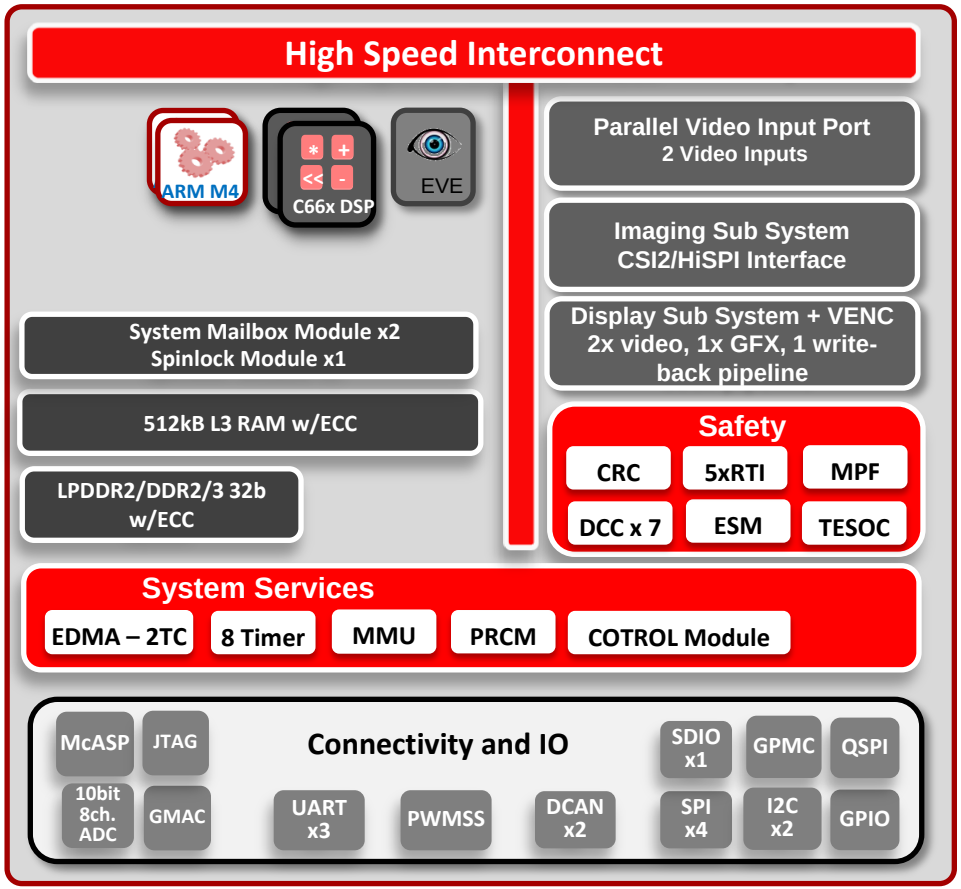
- **Two Next Generation DSP Cores: C66x™**
  - Upto 750 MHz – 12GMpy/s (16bx16b->32b)
  - Floating Point Extension / 24GFLOPs
- **Dual ARM Cortex™ A15 Cores**
  - Upto 750MHz – 5250DMIPs
  - NEON Vector Floating point
- **Two dual ARM Cortex™ M4 Cores**
  - 200 MHz
- **Four Vision Accelerator Cores: EVE**
  - Each core has an 16MAC per cycle computing engine with up to 650 MHz (8bit or 16bit) – 10.4GMACs per core
- **Video Codec Accelerator**
  - IVA-HD core running at up to 532MHz
- **Graphics Engine**
  - Dual SGX544 core delivering capability to render upto 166Mpoly/s / 5000MPixel/s / 31.9GFLOPs at 500Mhz
- **Internal Memory**
  - DSPs: each w/ 32 KB L1D, 32 KB L1P, unified 288 KB L2 Cache
  - ARM : 32 KB L1D, 32 KB L1P, combined 2 MB L2 Cache
  - On Chip L3 RAM: 2.5MB with ECC
- **Peripherals Highlights (1.8/ 3.3V IOs)**
  - Up to three Video input Ports(total of 10 parallel video inputs)
  - Display system Digital Video Output
  - Two EMIFs: 2x 32bit wide DDR2/3/3L @ 532MHz, one with ECC
  - GPMC: general purpose memory controller
  - Support for NOR Flash
  - PRU Subsystem
  - PCIe, Gbit EMAC with AVB support
  - 2x DCAN (High end CAN controller)
  - 10x UART, 5x I²C, 4x McSPI, Quad SPI, McASP, 15x Timers, WDT, GPIO



- **Package**
  - **23x23mm BGA (ABC)** -
  - **17x17mm BGA (AAS)** - reduced feature set

TDA3x scalable family (superset)

- **Two DSP Cores: C66x™**
  - Up to 750 MHz
  - Floating Point Extension
- **Dual ARM Cortex™ M4 Cores**
  - 200 MHz
- **Vision Accelerator Core: EVE**
  - Core has an 16MAC per cycle computing engine with up to 650 MHz (8bit or 16bit)
- **Image Signal Processer (ISP)**
  - 200 MHz, CSI/HiSPI
- **Internal Memory**
  - DSPs: each w/ 32 KB L1D, 32 KB L1P, unified 288 KB L2
  - ARM : 32 KB L1D, 32 KB L1P, 64kB L2 Cache
  - On Chip L3 RAM: up to 512kB with ECC
- **Peripherals Highlights (1.8/ 3.3V IOs)**
  - One Video input Port, with two 16 bit sub ports
  - Display system Digital Video Output including SD-DAC
  - One EMIF: 32bit wide DDR 2/3 or LPDDR 2 @ 400MHz with ECC
  - GPMC: general purpose memory controller
  - Support for NOR Flash
  - 2x Gbit EMAC with AVB support
  - 2x DCAN (High end CAN controller)
  - 3x UART, 2x I²C, 4x McSPI, Quad SPI, McASP, 8x Timers, GPIO
- **Safety Support**
  - 7 x Dual Clock Compare (DCC)
  - Error Signaling Module (ESM)
  - Run-Time BIST(TESOC)
  - CRC
  - 5xRTI
  - Memory Protection Firewall (MPF)



- **Power (~1.0V Core, 1.8/ 3.3V IOs)**
  - Target @ 125C Tj 1.5W at 500MHz 1x DSP & EVE, <1W at 250MHz 1x DSP & EVE. Power will vary depending on use case.
- **Package**
  - 15x15mm BGA, 0.65 mm ball pitch
  - 12x12mm BGA PoP, 0.65 mm ball pitch (offered up to 350MHz DSP/EVE)
  - Temperature Range: -40C to 125C Tj

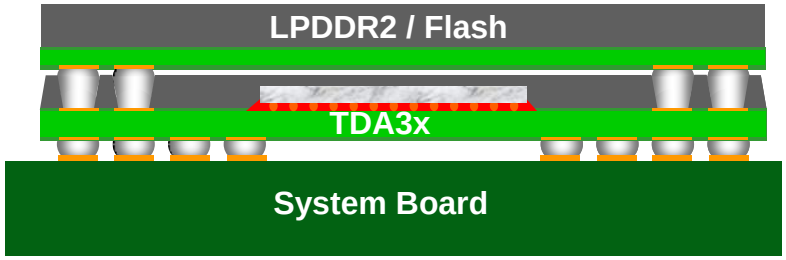
Key Feature Deltas Between TDAxxx Superset Devices

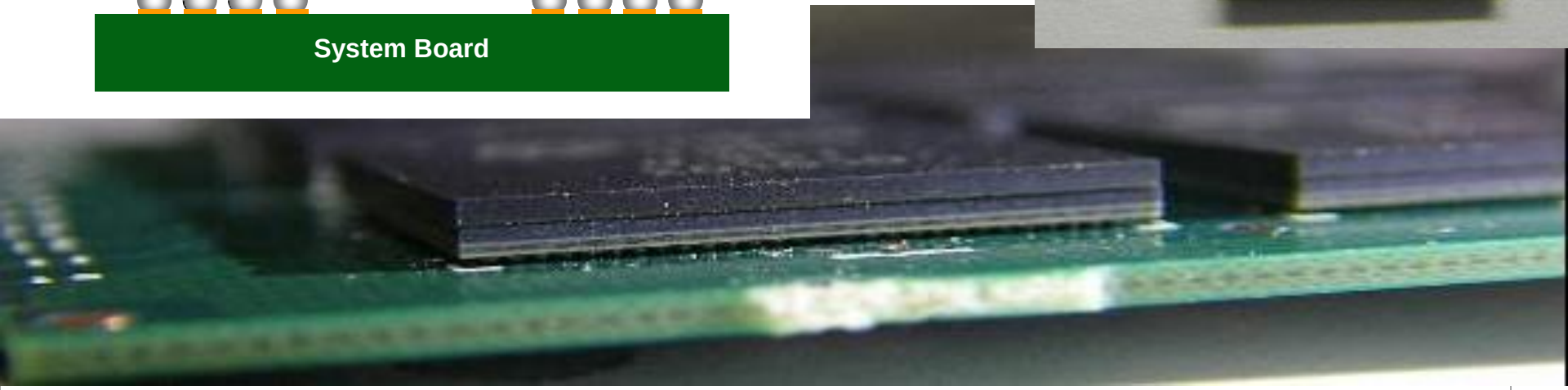
	Features	TDA2x	TDA3x
Processors	Cortex ARM A15	1..2 with 2MB of shared L2 cache	-
	Dual Cortex ARM M4	2	1
	C66x	1..2	1..2
	EVE	1..4	1
Video In	CSI2 Ports	-	One (1x 4 lane)
	Image Signal Processing (ISP)	-	Yes. (With LDC and HDR)**
	Parallel Video Inputs	Up to 10 parallel video inputs (6x12bit and 4x8bit)	Up to 4 video parallel inputs (4x8bit)
Peripherals	Internal On Chip Memory (L3 Memory)	2.5MB	512KB
	External Memory Interface 1	DDR3/3L 32 bit @533MHz (DDR2 @400MHz) w/ ECC	1x 32 bit w/ECC LPDDR2@400MHz OR DDR3/3L @532 MHz
	External Memory Interface 2	DDR3/3L 32 bit @533MHz (DDR2 @400MHz)	-
	Video Codec Accelerator	Yes (H.264, MJPEG etc.)	-
	Graphics	2x SGX544	-
	Display Subsystem	3 Digital Video Outputs (1GFX and 3 x VID Pipes)	1 Digital and 1 NTSC/PAL Out (1GFX and 2 x VID Pipes)
	Runtime Built in Self Test	-	Yes
	10-bit ADC	-	Yes
	I2C	5	2
	Package	23mm and 17mm	12mm POP and 15mm

**) Hardware accelerator for Pixel Remapping/Lens Distortion Correction and HDR available in 15mm package of TDA3x

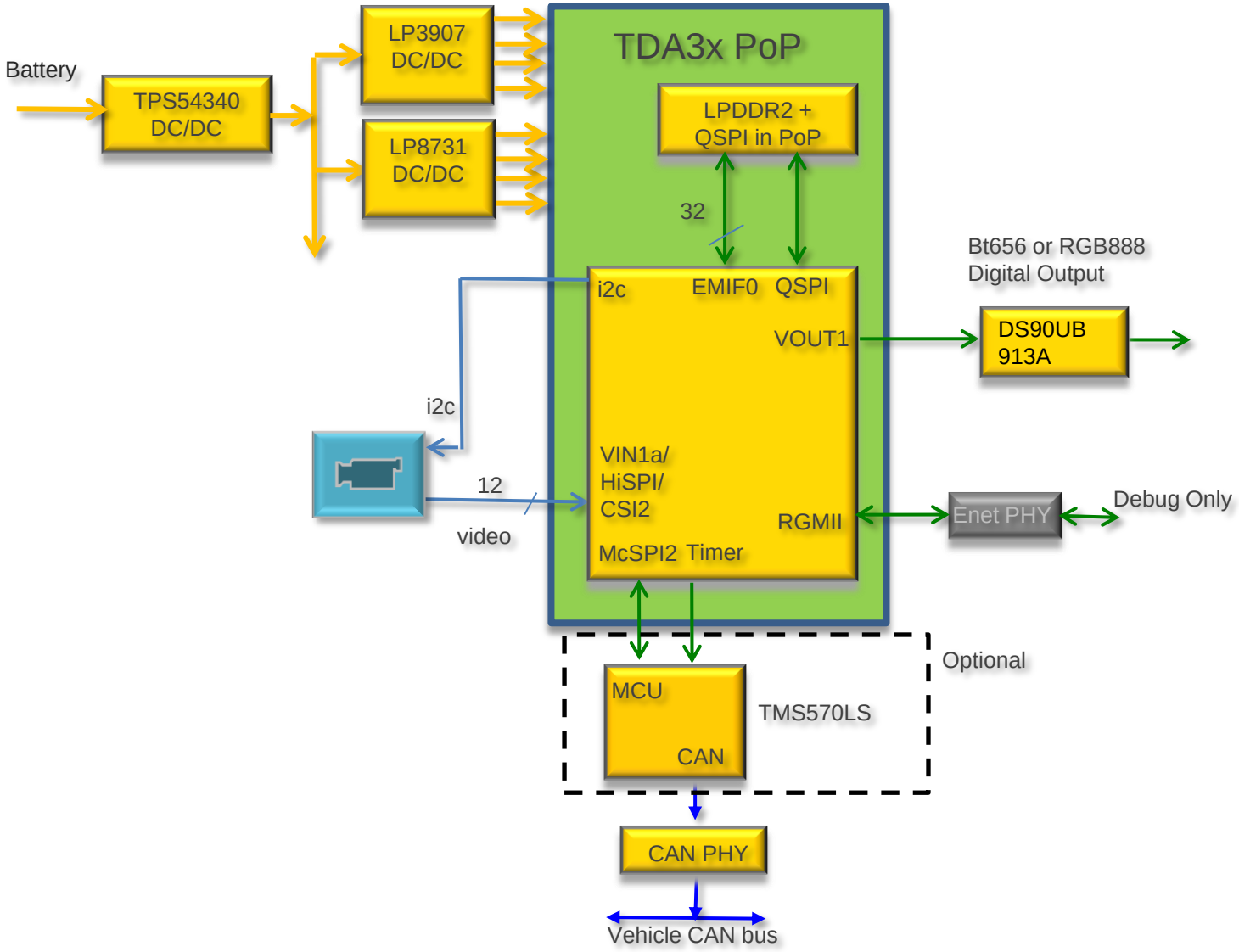
TDA3x POP Package Overview

- **Package on Package (PoP)**
  - POP for automotive study concluded with high confidence of meeting automotive requirements
  - TI has 10+ years of practical POP experience and >100M units shipped
- **PoP Advantages**
  - Lower cost memory:
  - Multiple memory suppliers mitigate supply risk
  - Supply continuity and Customer control

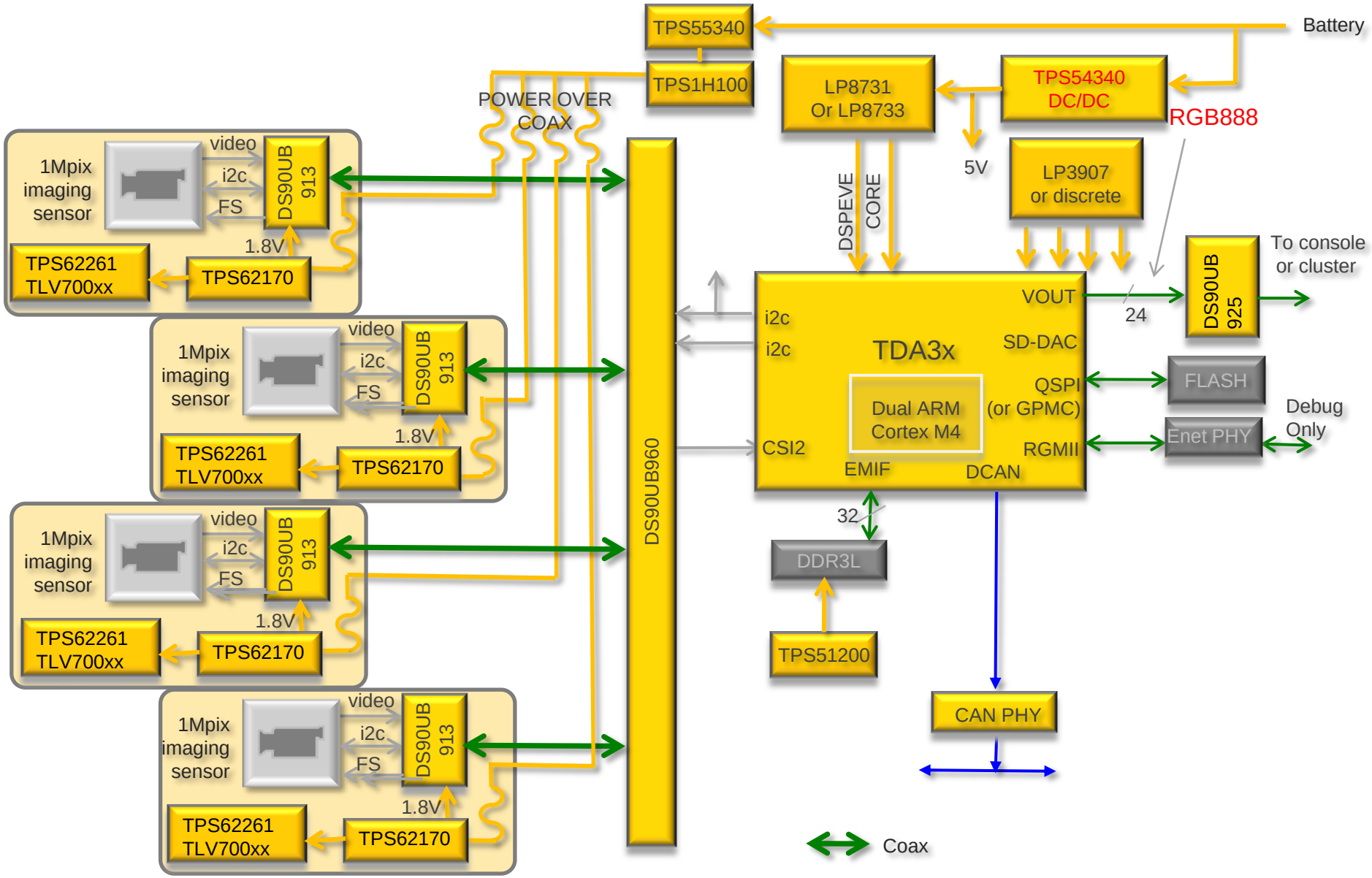




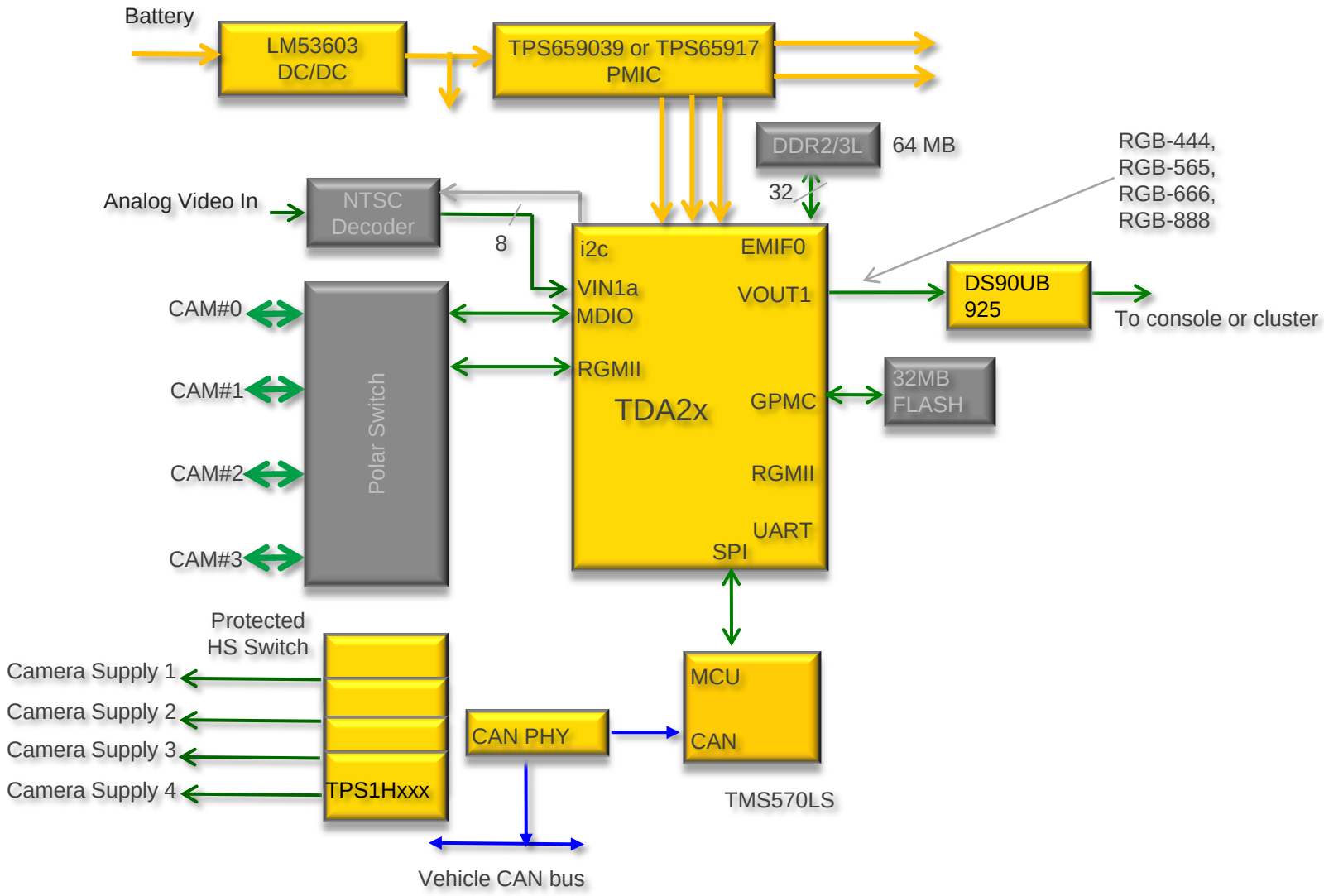
TDA3x Smart Rear View Camera – Digital Output



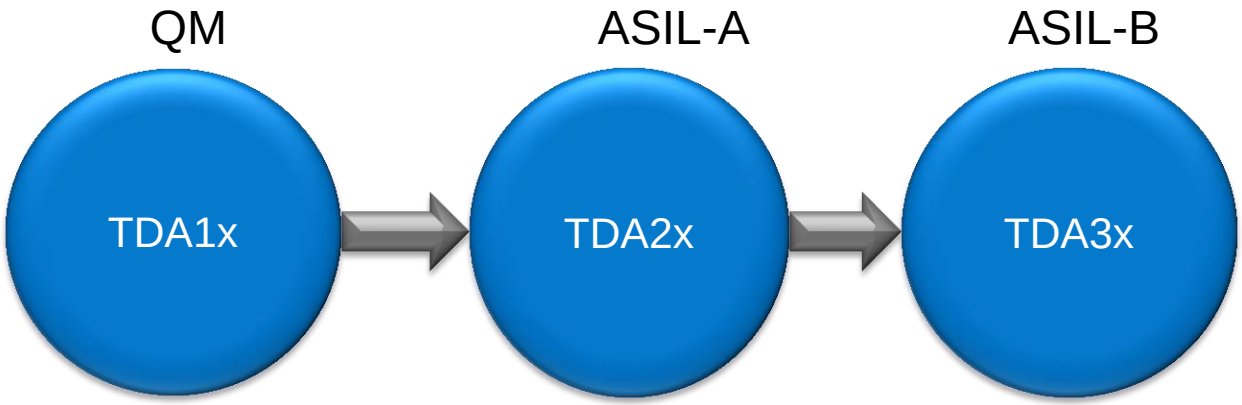
TDA3x LVDS Surround View (w/o External MCU)



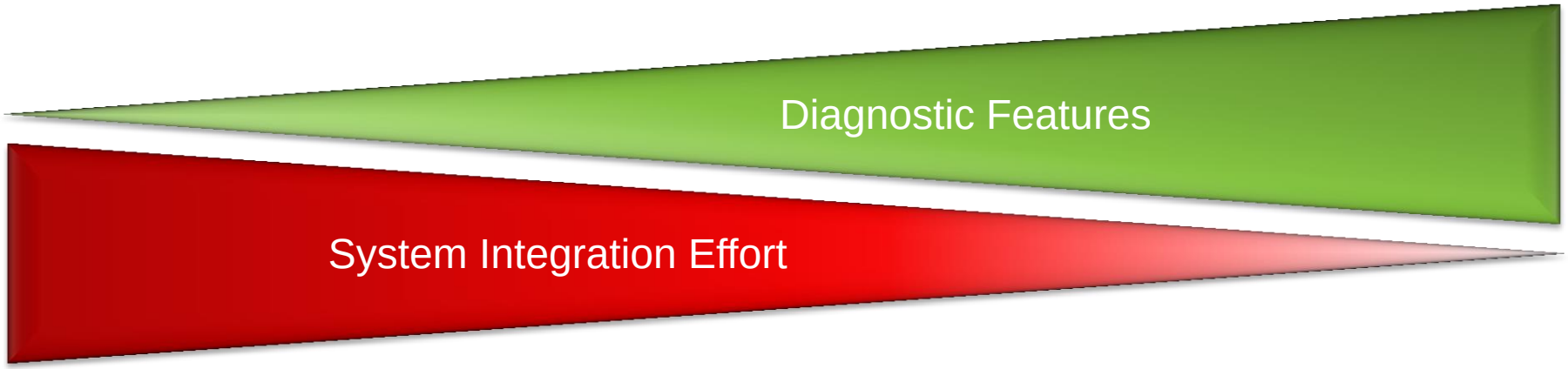
TDA2 Ethernet Surround View-High Level Block Diagram



Safety Evolution of TI SOCs



ISO26262 Compliant
Development Flow

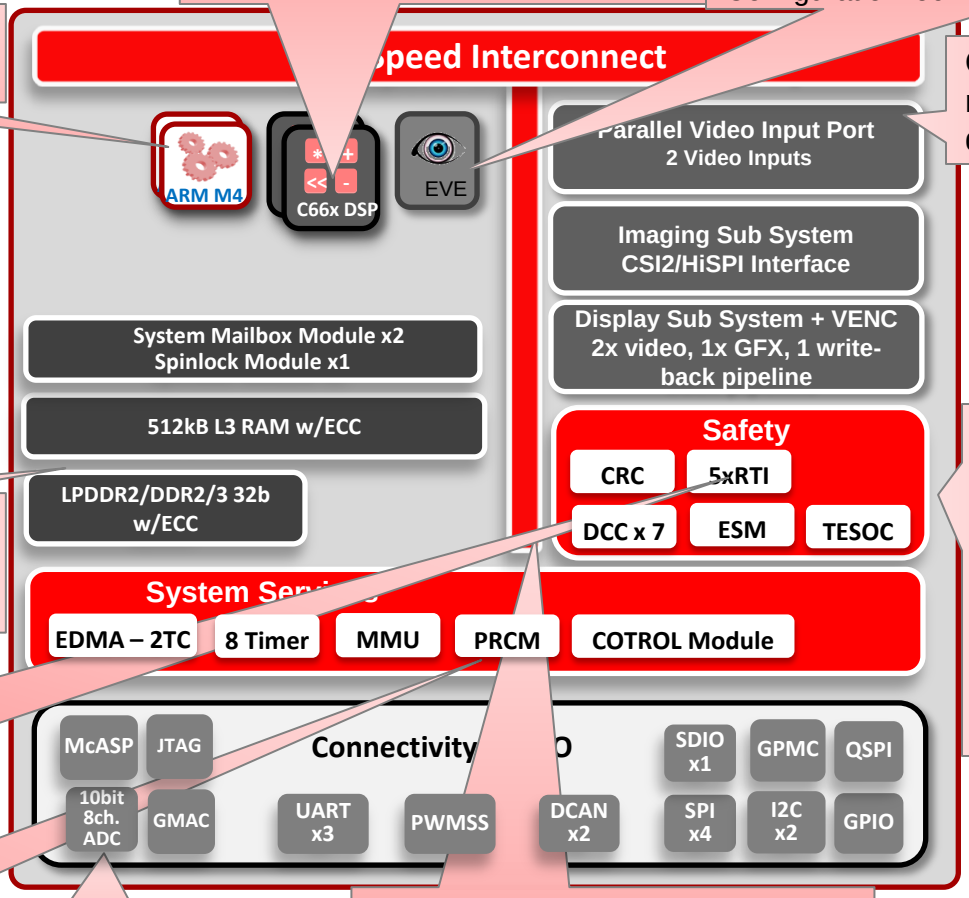


Overview of functional safety and diagnostic mechanisms for TDA3x

2 DSPs for redundant calculations
Parity on L1P $, SECDED on L2 $
Page based memory protection
Privilege modes and MMU to ensure "freedom from interference"

EVE Engines -
Error detection in vector core & interrupt generation
Undefined instruction trap on scalar core
Memory parity errors detection as well as an MMU
Configuration lock mechanisms and CRC self test

Fully ECC protected M4 subsystem



Overflow detection mechanisms for video and display ports

SECDED protection of Internal L3 RAM and External Memory Interface

Additional Safety features
Clock monitoring
Error Signaling Module
Voltage monitoring
Interrupt routing to off-chip CRC engines
On chip PBIST and LBIST
Temperature sensing

Window Watchdog functions
Message passing through mailbox
Multiple timers for consistency and redundancy

CLKOUT from PLL to off chip
Multiple clock, and power domains to avoid common cause fails

S/W diagnostic based voltage monitoring for core voltages

<u>Interconnect safety features</u>
Firewalls to ensure memory isolation
Error handling and abort interrupts
Timeout mechanisms
Statistics and perf monitor module
Bandwidth regulation
Ability to run s/w defined diagnostics

Power Dissipation Estimates for TDAx SoC – at Tj=105C

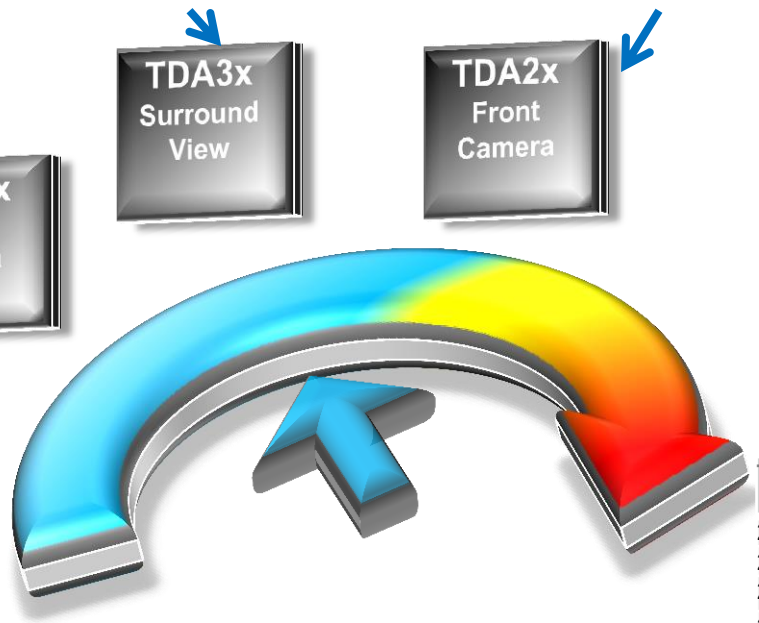
Tj=105C	Frequency [MHz]	Utilization [%]
2xC66x	500	80
1xEVE	500	80
CortexM4	212	80
ISS+CSI2	200	80
TOTAL POWER	**1.7 W**	

Tj=105C	Frequency [MHz]	Utilization [%]
2xC66x	500	80
2xEVE	500	80
1xCortex A15	500	80
CortexM4	212	80
VIP1	100	
TOTAL POWER	**2.3 W**	

Tj=105C	Frequency [MHz]	Utilization [%]
2xC66x	500	80
1xEVE	500	80
CortexM4	212	80
VIP1	100	
TOTAL POWER	**1.3 W**	

Tj=105C	Frequency [MHz]	Utilization [%]
1xC66x	250	80
1xEVE	250	80
CortexM4	212	80
ISS+CSI2	200	80
TOTAL POWER	**1.1 W**	

Tj=105C	Frequency [MHz]	Utilization [%]
2xC66x	500	80
2xEVE	500	80
2xCortex A15	1176	80
2xICSS	200	100
GMAC_SW	125	100
TOTAL POWER	**4.4W**	



NOTES:

- All Power Estimates Assume Tj of 105 °C and Use of Smart Reflex (Adaptive Voltage Scaling).
- Assumed 80% Utilization for Compute Cores (C66x and EVE) is very conservative.
- Power figures shown represent a rough estimate based on a hypothetical use cases. For more accurate power dissipation estimate a precise description of target use case is required (list of all used IPs along with their utilization and clock frequencies, DDR type, DDR data width, DDR frequency and data-throughput).

ADAS Applications –SoC & SW

Core Applications

Front Camera

Scalable Performance
Low Power
Safety

TDA2x

- Vision SDK
- Framework
- DSP/EVE Libs
- Starterware
- AutoSAR MCAL

TDA3x

- Vision SDK
- Framework
- DSP/EVE Libs
- Starterware
- Diagnostics Libs
- AutoSAR MCAL
- ISP Tuning Tool
- ISP Example Algos/Drivers

Rear Camera

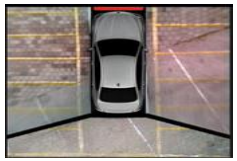
Low Power
Small Footprint
Scalable Analytics

TDA3x

- Vision SDK
- Framework
- DSP/EVE Libs
- Starterware
- Diagnostics Libs
- AutoSAR MCAL
- ISP Tuning Tool
- ISP Example Algos/Drivers

Surround View Park Assist

Integrate 2D/3D Graphics
Scalable Analytics
Security



TDA2x

- Linux SDK -> InfoADAS Package
- Vision SDK
- Framework
- DSP/EVE Libs
- Starterware
- AutoSAR MCAL

TDA3x

- Vision SDK
- Framework
- DSP/EVE Libs
- Starterware
- ISP Tuning Tool
- ISP Example Algos/Drivers
- Diagnostics Libs
- AutoSAR MCAL

Radar

Scalable performance
MCU Integration
Safety

TDA3x

- Vision SDK
- Framework
- DSP/EVE Libs
- Starterware
- Diagnostics Libs
- AutoSAR MCAL

Vision SDK

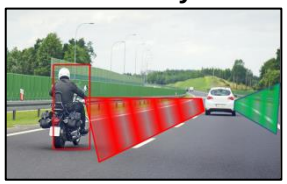
One SDK spanning all Processors & Applications
Enables scalable SW development

ADAS Applications –SoC & SW

Emerging Applications

Sensor Fusion

Performance
Safety
Security



TDA2x
Fusion

- Vision SDK
  - Framework
  - DSP/EVE Libs
  - Starterware
  - Diagnostics Libs
  - AutoSAR MCAL

Driver Monitoring

Small Footprint
ISP Integration Scalable
Analytics

TDA3x

- Vision SDK
  - Framework
  - DSP/EVE Libs
  - Starterware
  - Diagnostics Libs
  - ISP Tuning Tool
  - ISP Example Algos/Drivers
  - AutoSAR MCAL

Mirror Replacement

Performance
ISP Integration
Scalable Analytics

TDA3x

- Vision SDK
  - Framework
  - DSP/EVE Libs
  - Starterware
  - Diagnostics Libs
  - ISP Tuning Tool
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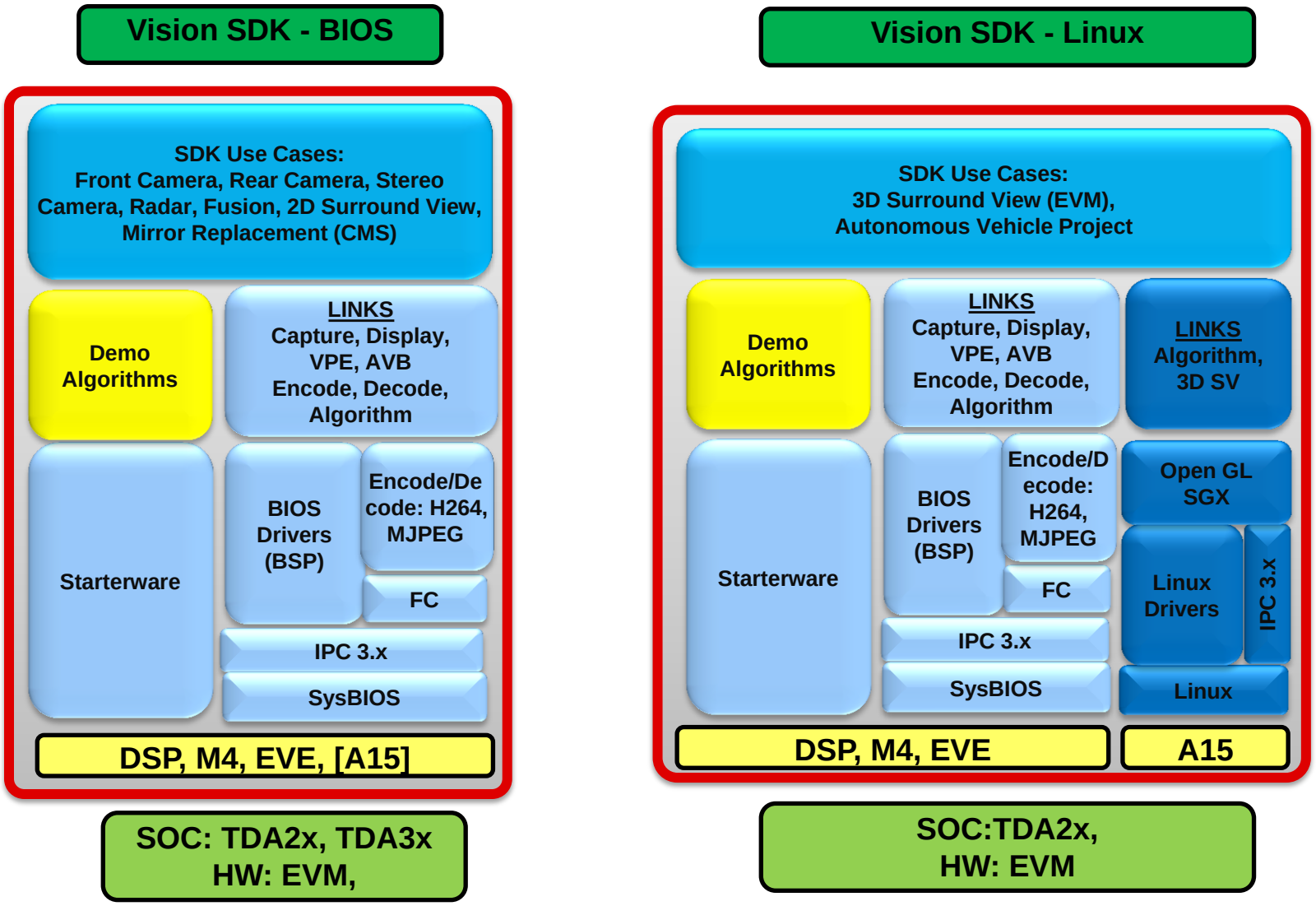
  - AutoSAR MCAL

Vision SDK

One SDK spanning all Processors & Applications
Enables scalable SW development

ADAS Vision SDK: Two Flavors



Conclusions

- Continuous demand for performance increase in ADAS systems is in conflict with miniaturization of the camera module, use of plastic enclosures and cost reduction.
- It has been shown that given the diverse compute requirements for the various algorithms in ADAS functions, a heterogeneous multicore architecture like the TI TDA2x/3x SOC platform is required to provide a scalable ADAS system solution.
- Further, functional safety and compliance to ISO26262 standard is an orthogonal requirement that has to be satisfied for systems implementing ADAS functions.

Thank You

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